CLAIMS:

1.   A method of operating a direct sequence code division
multi-access transmitter, the method comprising the steps
of:

5   reading   a   series   of   bits   that   includes   a   first
plurality   of   bits   having   a   first   value   and   a   second
plurality of bits having a second value; and
          selectively transmitting a first direct sequence code
          in response to each of the first plurality of bits.

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2.   The method according to claim 1 further comprising the
step of:
          selectively interrupting a radio frequency transmission
in response to each of the second plurality of bits.

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3.   The method according to claim 1 wherein the step of
selectively transmitting the first direct sequence includes
the sub-step of:
          modulating a carrier frequency with the first direct
20   sequence code.

4.   The method according to claim 3 wherein the sub-step of
modulating a carrier frequency with the first direct
sequence code includes the sub-step of:
25   binary phase shift key modulating the carrier with the
first direct sequence code.

5.   The method according to claim 3 further comprising the
step of:

selectively ceasing modulation of the carrier frequency in response to each of the second plurality of bits.

6. The method according to claim 1 further comprising the
5 step of:
   selectively transmitting a second direct sequence code in response to each of the second plurality of bits.

7. The method according to claim 6 wherein the step of
10 selectively transmitting the the direct sequence includes the sub-step of:
   modulating a carrier frequency with the second direct sequence code.

15 8. The method according to claim 7 wherein the sub-step of modulating a carrier frequency with the second direct sequence code includes the sub-step of:
   binary phase shift key modulating the carrier with the second direct sequence code.

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9. A method of receiving information using a direct sequence code division multi-access receiver, the method comprising the steps of:

5   receiving a first signal that includes one or more direct sequence codes;

sampling the signal to obtain a series of complex chip values;

multiplying each Nth complex chip value in the
10   series, by the complex conjugate of another complex chip value in the series that is separated from the Nth complex chip value by a predetermined number of places to obtain a differentially decoded series;

performing a vector dot product between a
15   plurality of bit length sub-series selected from the differentially decoded series, and a reference vector to obtain a series of dot product values; and

comparing each of the series of dot product values to one or more predetermined constants.

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10. The method according to claim 9 wherein the step of multiplying comprises the sub-step of:

multiplying each Nth complex chip value in the series, by the complex conjugate of a another complex
25   chip value in the series that is adjacent to the Nth complex chip value to obtain the differentially decoded series.

11. The method according to claim 9 wherein the step of
30   receiving a first signal comprises the sub-step of:

receiving a signal consisting of multiple copies of a single direct sequence code interspersed with null periods.

12   The method according to claim 11 wherein the step of

5   performing a dot product includes the sub-step of:

performing a vector dot product between a plurality of bit length sub-series selected from the differentially decoded series, and a reference vector that is equal to a vector obtained by multiplying each Nth element in the

10   single direct sequence code, by another element in the single direct sequence code that is separated from the Nth element by the predetermined of places number, to obtain a series of dot product values.

15   13.   The method according to claim 12 wherein the step of comparing each of the series of dot product values to one or more predetermined constants includes the sub-step of:

comparing each of the series of dot product values to a first constant.

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14.   The method according to claim 9 wherein the step of receiving a first signal that includes one or more direct sequence codes comprises the sub-step of:

receiving a signal that includes a first direct

25   sequence code and a second direct sequence code.

15.   The method according to claim 14 wherein the step of performing a dot product includes the sub-step of:

performing a vector dot product between a plurality of

30   bit length sub-series selected from the differentially

decoded series, and a reference vector that is substantially equivalent to a vector obtained by subtracting a first component vector that is obtained multiplying each Nth element in the first direct sequence code, by another

5   element in the first direct sequence code that is separated from the Nth element in the first direct sequence code by the predetermined number from a second component vector that is obtained multiplying each Nth element in the second direct sequence code, by another element in the second

10   direct sequence code that is separated from the Nth element in the second direct sequence code by the predetermined number, to obtain a series of dot product values.

16   The method according to claim 15 wherein the step of

15   comparing each of the series of dot product values to one or more predetermined constants includes the sub-step of:

comparing each of the series of dot product values to a constant that is about zero.

20   17.   The method according to claim 9 wherein the step of receiving a first signal that includes one or more direct sequence codes comprises the sub-step of:

receiving a signal that includes 2^N distinct direct sequence codes, where N is an integer.

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18.   The method according to claim 17 further comprising the step of:

obtaining the reference vector that is equal to a vector obtained by:

processing each distinct direct sequence code by multiplying each Nth element in the distinct direct sequence code, by another element in the distinct direct sequence code that is separated from the Nth

5   element by the predetermined number, to obtain 2^N distinct differentially decoded vectors;

multiplying each distinct differentially decoded vector by a distinct constant to obtain a plurality of component vectors; and

10   summing the component vectors.

19.   The method according to claim 18 wherein the step of comparing each of the series of dot product values to one or more predetermined constants comprises the sub step of:

15   comparing each of the series of dot product values to a plurality of distinct constants.

20.   The method according to claim 9 wherein the step of receiving the first signal that includes one or more direct

20   sequence codes comprises a sub-step of:

in-phase and quadrature demodulating a received RF signal to obtain a complex demodulator output signal;

low pass filtering the complex demodulator output signal to obtain the first signal.

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21.   The method according to claim 20 wherein the step of low pass filtering comprises the sub-step of:

filtering the demodulator output with a chip pulse match filter.

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22. The method according to claim 9 wherein the step of receiving a first signal comprises the sub-step of:

     receiving a signal that includes a direct sequence code having at least about seven elements

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23 The method according to claim 9 wherein the step of receiving a first signal comprises the sub-step of:

     receiving a signal that includes a direct sequence code having at least about 15 elements

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24.   A direct sequence code division multi-access
transmitter comprising:

a bit value decoder for receiving binary data that
includes a first plurality of bits having a first value

5   and a second plurality of bits having a second value at
a decoder input, and selectively outputting a first
direct sequence code in response to each of the first
plurality of bits, at a first decoder output;

a pulse shaper coupled to the bit value decoder

10   for receiving the first direct sequence code and
outputting a baseband signal including the first direct
sequence code at a pulse-shaper output;

a modulator including:

a signal input coupled the pulse shaper

15   output for receiving the baseband signal;

a carrier frequency input; and

an RF output;

a carrier frequency source including a source
output coupled to the carrier frequency input of

20   the modulator; and

an antenna coupled to the RF output of the
modulator.

25.   The direct sequence code division multi-access

25   transmitter according to claim 24 further comprising:

an amplifier including:

a signal input coupled to the modulator,

an amplified signal output coupled to the
antenna;

30   an a control input; and

the bit value decoder further comprises a second
decoder output for coupled to the control input for
selectively turning off the amplifier in response to the
second plurality of bits.

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26. The direct sequence code division multi-access
transmitter according to claim 24 wherein the bit value
decoder comprises:

a processor programmed to:

10   read the binary data; and

selectively output the first direct sequence
code only upon reading a bit having the first
value.

15   27. The direct sequence code division multi-access
transmitter according to claim 24 wherein the decoder
comprises:

a bit value decoder for receiving binary data that
includes a first plurality of bits having a first
20   value and a second plurality of bits having a
second value at a decoder input, and selectively
outputting a first direct sequence code in
response to each of the first plurality of bits,
at the first decoder output, and selectively
25   outputting a second direct sequence code in
response to each of the second plurality of bits.

28. The direct sequence code division multi-access
transmitter according to claim 27 wherein the decoder
30   comprises:

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a processor programmed to:

    read the binary data; and

    selectively output the first direct sequence code upon reading each of the first plurality of bits, and selectively output the second direct sequence code upon reading each of the second plurality of bits.

29. A direct sequence code division multi-access
information receiver comprising:
        a channel interface for receiving a signal including a
5   sequence of complex chip values;
        a multiplier for multiplying each Nth chip value in the
sequence of chip values by the complex conjugate of another
chip value in the sequence of chip values that is separated
from the Nth by a predetermined number of places to obtain
10 one or more chip-by-chip differentially decoded sequences;
        a dot product performer for performing a dot product
between the one or more chip-by-chip differentially decoded
sequences and a one or more reference vectors and outputting
one or more dot product values; and
15   a discriminator for identifying one or more information
conveying symbols based on the one or more dot product
values.

30. The direct sequence code division multi-access
20 information receiver according to claim 29 wherein the
channel interface comprises:
        an antenna for receiving an RF signal;
        a I/Q demodulator coupled to the antenna for receiving
the RF signal and outputting a complex demodulated signal;
25   a low pass filter coupled to the demodulator for
receiving the complex demodulated signal, and outputting a
complex baseband signal; and
        an analog-to-digital converter coupled to the low pass
filter for sampling the complex baseband signal to obtain
30 the sequence of complex chip values.

31.   The direct sequence code division multi-access information receiver according to claim 29 wherein the multiplier comprises:

5   a processor programmed to:

multiply each Nth complex chip value in the sequence of complex chip values by the complex conjugate of another complex chip value in the sequence of chip values that is separated from the Nth by a

10   predetermined number of places.

32.   The direct sequence code division multi-access information receiver according to claim 29 wherein the dot product performer comprises:

15   a processor programmed to:

compute one or more dot products between the one or more chip-by-chip differentially decoded sequences and a one or more reference vectors and outputting one or more dot product values.

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33.   The direct sequence code division multi-access information receiver according to claim 29 wherein the discriminator comprises:

a comparator for comparing the one or more dot product

25   values to one or more constants that are associated with the one or more information carrying symbols.

34.   The direct sequence code division multi-access information receiver according to claim 29 wherein the dot

30   product performer comprises:

a dot product performer for performing a dot product between the one or more chip-by-chip differentially decoded sequences and a reference vector that includes a first pseudo noise sequence that is associated with a first

5   information symbol , vectorially added to a second pseudo noise sequence that is associated with a second information symbol and outputting one or more dot product values.

35.   The direct sequence code division multi-access

10   information receiver according to claim 29 wherein:

the dot product performer comprise a dot product performer for performing a dot product between the one or more chip-by-chip differentially decoded sequences and a single reference vector and outputting one or

15   more dot product values; and

the discriminator comprises a comparator for comparing each of the one or more dot product values to a threshold value, and outputting a first bit value in the case that a dot product value exceeds the

20   threshold.

36.   The direct sequence code division multi-access information receiver according to claim 29 wherein the multiplier comprises:

25   a multiplier for multiplying each chip value in the sequence of chip values by the complex conjugate of an adjacent chip value in the sequence of chip values to obtain one or more chip-by-chip differentially decoded sequences.

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37.   A direct sequence code division multi-access
communication system comprising:
      a transmitter equipped communication device including:

5   a decoder for receiving binary data that includes
a first plurality of bits having a first value and a
second plurality of bits having a second value at a
decoder input, and selectively outputting a first
direct sequence code that includes a plurality of

10   elements, in response to a first bit pattern, at a
decoder output; and
      a first channel interface for transmitting a
signal including the first direct sequence code; and
      a receiver equipped communication device

15   including:
          a second channel interface for receiving the
      signal including the first direct sequence code;
          a sampler for sampling the signal to obtain a
      first sequence of complex chip values;

20   a multiplier for multiplying each Nth chip
      value in the first sequence of chip values by the
      complex conjugate of a second chip value in the
      first sequence of chip values that is separated
      from the Nth by a predetermined number of places

25   to obtain one or more chip-by-chip differentially
      decoded sequences;
          a dot product performer for performing a dot
      product between the one or more chip-by-chip
      differentially decoded sequences and a one or more

reference vectors and outputting one or more dot

product values; and

    a discriminator for identifying one or more

information conveying symbols based on the one or more

5   dot product values.

38.   The direct sequence code division multi-access

communication system according to claim 37 wherein:

    the first channel interface comprises:

10   a pulse shaper for receiving the first direct

sequence code at a first input and outputting a

baseband signal including the first direct

sequence code;

    a modulator including:

15   a signal input coupled the pulse shaper

for receiving the baseband signal;

    a carrier frequency input; and

    an RF output;

    a carrier frequency source coupled to the

20   carrier frequency input of the modulator;

    an amplifier having an input coupled to the

RF output of the modulator, and an amplifier

output; and

    an antenna coupled to the amplifier output.

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39   The direct sequence code division multi-access

communication system according to claim 37 wherein:

    the decoder is configured for receiving binary

data that includes a first plurality of bits having a

30   first value and a second plurality of bits having a

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second value at a decoder input, selectively outputting
the first direct sequence code in response to a first
bit pattern, and selectively outputting a second direct
sequence code in response to a second bit pattern.

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40.   A computer readable medium having stored thereon a
despreading code comprising:

a vector sum of:

5   a differentially decoded version of a first
pseudo noise number, wherein the first pseudo
noise number is used to represent a first
information symbol; and

a differentially decoded version of a second
10   pseudo noise number, wherein the second pseudo
noise number is used to represent a second
information symbol.

41. A despreading code embodied in a carrier wave, the despreading code comprising:

a vector sum of:

5   a differentially decoded version of a first pseudo noise number, wherein the first pseudo noise number is used to represent a first information symbol; and

a differentially decoded version of a second

10   pseudo noise number, wherein the second pseudo noise number is used to represent a second information symbol.

42.   A computer readable medium having programming
instructions for operating a direct sequence code division
multi-access transmitter, including programming instructions

5   for:

          reading a series of bits that includes a first
     plurality of bits having a first value and a second
     plurality of bits having a second value; and
          selectively transmitting a first direct sequence

10   code in response to each of the first plurality of
     bits.

43.   The computer readable medium according to claim 42
further comprising programming instructions for:

15   selectively interrupting a radio frequency
          transmission in response to each of the second
          plurality of bits.

44   A computer readable medium having programming
instruction for operating a direct sequence code division
multi-access receiver, including programming instructions
5   for:

     reading a series of complex chip values;

     multiplying each Nth complex chip value in the
series, by the complex conjugate of another complex
chip value in the series that is separated from Nth
10   complex chip value by a predetermined number of places
to obtain a differentially decoded series;

     performing a vector dot product between a
plurality of bit length sub-series selected from the
differentially decoded series, and a reference vector
15   to obtain a series of dot product values; and

     comparing each of the series of dot product values
to one or more predetermined constants